



2013 International SoC Design Conference

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CDC(D)-001	Multiple-Output Switched-Capacitor DC-DC Converter with Digital Capacitance Modulation	Jeongyun Lee, Sunwoo Yoon and Donghyun Baek <i>Chung-Ang University, Korea</i>	172
CDC(D)-002	A 5.6Gb/s CMOS CDR IC with a static phase offset compensated linear phase detector	Chung Hwan Son and Sangjin Byun <i>Dongguk University, Korea</i>	178
CDC(D)-003	A 12 Gb/s 0.92mW/Gb/s Forwarded Clock Receiver with Low Jitter tracking Bandwidth Variation in 65nm CMOS	Young-Ju Kim and Lee-Sup Kim <i>Korea Advanced Institute of Science and Technology(KAIST), Korea</i>	179
CDC(D)-004	Effect of Signal Selection Algorithm on the FPN Characteristics in a Two Step Charge Transfer Linear-logarithmic APS	Inkyu Baek, Jiwon Lee, Seungmin Baek and Kyoungsoon Yang <i>Korea Advanced Institute of Science and Technology(KAIST), Korea</i>	180
CDC(D)-005	A C-band Bi-directional T/R Chipset in 0.18 μm CMOS Technology	Moon-Kyu Cho, Jang-Hoon Han, Jin-Hyun Kim and Jeong-Geun Kim <i>Kwangwoon University, Korea</i>	181
CDC(D)-006	Census Transform Based Stereo Matching Accelerator	Hyeon-Sik Son, Kyeong-ryeol Bae, Seung-Ho Ok and Byungin Moon <i>Kyungpook National University, Korea</i>	182
CDC(D)-007	Design of multimedia system with Core-A processor	Seungpyo Jung and Jusung Park <i>Pusan National University, Korea</i>	183
CDC(D)-008	A Fully-Integrated Low Power 24 GHz Radar Transceiver using 110nm CMOS Process	Hyung-Jun Cho, Seong-Kyun Kim, Chenglin Cui and Byung-Sung Kim <i>Sungkyunkwan University, Korea</i>	184
CDC(D)-009	A Design of 77GHz LNA Using 65nm CMOS Process	Jun-Young Kim, Seong-Kyun Kim, Chenglin Cui and Byung-Sung Kim <i>Sungkyunkwan University, Korea</i>	185
CDC(D)-010	Design of 77GHz receiver using on-chip waveguide feeder in 65 nm CMOS	Hyeong-Ki Nam, Hyun-Sang Kang, Seong-Kyun Kim, Chenglin Cui and Byung-Sung Kim <i>Sungkyunkwan University, Korea</i>	186
CDC(D)-011	An 8.7-mW 7-Gb/s CMOS OEIC Receiver	Jin-Sung Youn, Myung-Jae Lee, Wang-Soo Kim, Kang-Yeob Park and Woo-Young Choi <i>Yonsei University, Korea</i>	187
CDC(D)-012	A HW-SW Co-Design For A Real-Time Spectral Subtraction Based Noise Cancellation System		

An 8.7-mW 7-Gb/s CMOS OEIC Receiver

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I. INTRODUCTION

High-performance optoelectronic integrated circuit (OEIC) receivers in CMOS technology have been actively investigated for 850-nm short-distance optical interconnect applications [1-2]. For these applications, low-power operation is strongly required. We present a 7-Gb/s OEIC receiver having an 850-nm Si avalanche photodetector (APD) realized in 65-nm CMOS technology. Our receiver achieves power efficiency of 1.24 mW/Gb/s.

II. DESCRIPTION

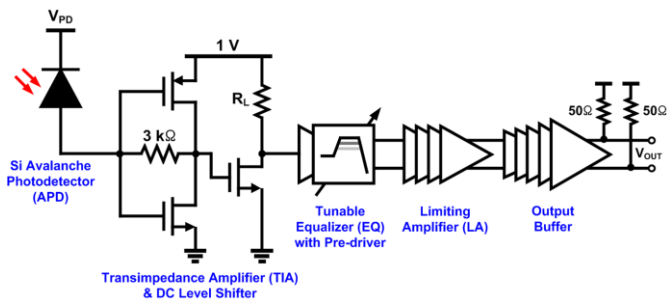


Fig. 1. Simplified block diagram of our CMOS OEIC receiver.

Fig. 1 shows the block diagram of our OEIC receiver. It is composed of a Si APD, a transimpedance amplifier (TIA) with a DC level shifter, a tunable equalizer (EQ) with a single-to-differential amplifier, a limiting amplifier (LA), and an output buffer with 50-Ω loads. The Si APD is implemented with P⁺/N-well junction surrounded by shallow trench isolation [3], and its optical-window size is about 10 μm by 10 μm. The TIA is composed of an inverter-based amplifier and a feedback resistance of 3 kΩ. The inverter-based amplifier can provide much lower power consumption compared to CML-type amplifiers, but in 65-nm CMOS technology its operation speed is limited to about 3 GHz. Single-ended signals at TIA output are converted into fully differential signals with the DC level shifter and the single-to-differential amplifier. The tunable EQ is composed of two-stage of identical cells, and each cell has a differential amplifier with source degeneration and negative capacitance. The LA is composed of four-stage gain cells, and each gain cell is composed of two-stage differential amplifiers with active feedback. The output buffer is used for driving 50-Ω loads.

III. CHIP IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 2 shows the chip photograph of the fabricated OEIC receiver in 65-nm CMOS technology. The chip area is about 480 μm by 140 μm. The total power consumption excluding output buffer is about 8.7 mW with 1-V supply voltage.

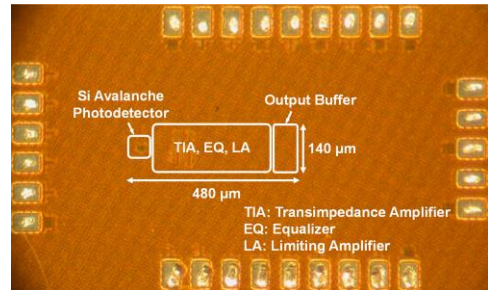


Fig. 2. Chip photograph of the fabricated CMOS OEIC Receiver.

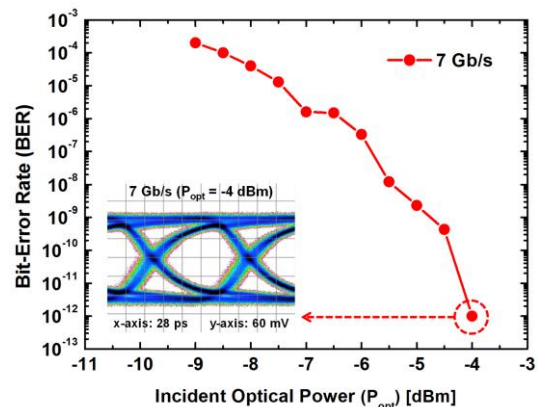


Fig. 3. Measured bit-error rate performance versus incident optical power (P_{opt}). Inset shows the measured 7-Gb/s eye diagram.

With the fabricated CMOS OEIC receiver, 7-Gb/s (PRBS 2³¹-1) 850-nm optical data were successfully detected. Fig. 3 shows the measured bit-error rate performance as a function of incident optical power. The inset in Fig. 3 shows the measured eye diagram. Compared to other 850-nm CMOS OEIC receivers reported so far, our receiver has the lowest power efficiency (This work: 1.24 mW/Gb/s, [1]: 6.68 mW/Gb/s, [2]: 11.8 mW/Gb/s).

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