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An 8.7-mW 7-Gb/s CMOS OEIC Receiver

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I. INTRODUCTION

High-performance optoelectronic integrated circuit (OEIC) receivers in CMOS technology have been actively investigated for 850-nm short-distance optical interconnect applications [1-2]. For these applications, low-power operation is strongly required. We present a 7-Gb/s OEIC receiver having an 850-nm Si avalanche photodetector (APD) realized in 65-nm CMOS technology. Our receiver achieves power efficiency of 1.24 mW/Gb/s.

II. DESCRIPTION

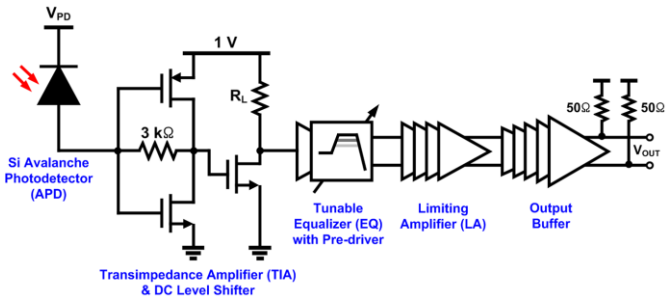

Fig. 1. Simplified block diagram of our CMOS OEIC receiver.

Fig. 1 shows the block diagram of our OEIC receiver. It is composed of a Si APD, a transimpedance amplifier (TIA) with a DC level shifter, a tunable equalizer (EQ) with a single-to-differential amplifier, a limiting amplifier (LA), and an output buffer with 50-Ω loads. The Si APD is implemented with P^+/N-well junction surrounded by shallow trench isolation [3], and its optical-window size is about 10 µm by 10 µm. The TIA is composed of an inverter-based amplifier and a feedback resistance of 3 kΩ. The inverter-based amplifier can provide much lower power consumption compared to CML-type amplifiers, but in 65-nm CMOS technology its operation speed is limited to about 3 GHz. Single-ended signals at TIA output are converted into fully differential signals with the DC level shifter and the single-to-differential amplifier. The tunable EQ is composed of two-stage of identical cells, and each cell has a differential amplifier with source degeneration and negative capacitance. The LA is composed of four-stage gain cells, and each gain cell is composed of two-stage differential amplifiers with active feedback. The output buffer is used for driving 50-Ω loads.

III. CHIP IMPLEMENTAION AND MEASUREMENT RESULTS

Fig. 2 shows the chip photograph of the fabricated OEIC receiver in 65-nm CMOS technology. The chip area is about 480 µm by 140 µm. The total power consumption excluding output buffer is about 8.7 mW with 1-V supply voltage.

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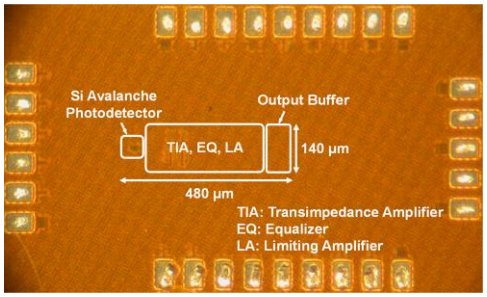

Fig. 2. Chip photograph of the fabricated CMOS OEIC Receiver.

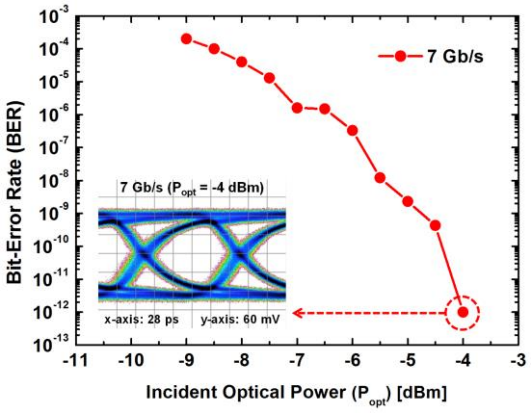

Fig. 3. Measured bit-error rate performance versus incident optical power (P_{opt}). Inset shows the measured 7-Gb/s eye diagram.

With the fabricated CMOS OEIC receiver, 7-Gb/s (PRBS 2^{31}-1) 850-nm optical data were successfully detected. Fig. 3 shows the measured bit-error rate performance as a function of incident optical power. The inset in Fig. 3 shows the measured eye diagram. Compared to other 850-nm CMOS OEIC receivers reported so far, our receiver has the lowest power efficiency (This work: 1.24 mW/Gb/s, [1]: 6.68 mW/Gb/s, [2]: 11.8 mW/Gb/s).

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